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(54) Semiconductor packaging apparatus and method

(57) Semiconductor devices 340 are formed in semiconductor wafer 300. Contact pads 332 are formed in each die 330. An interconnect connects the contact pads 332 to die surface contact regions 210, 212. Scribe trenches 348 are formed in device wafer 300; corresponding trenches 358 are formed in cover wafer 360. The cover wafer 360 is thinned to open scribe trenches 348. Conductive vias 310-313 connect the contact pads 210, 212 to external surface bump contacts 333.

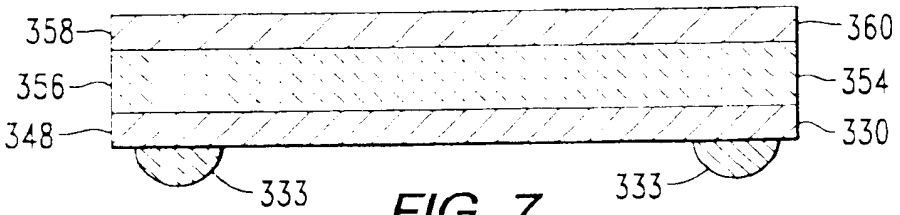

FIG. 7

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Description

The present invention relates to semiconductor device structures and methods for packaging such structures at the wafer level without requiring plastic encapsulation or enclosure in ceramic packages after the individual semiconductor devices (also known as dice) are formed.

The invention is suitable for sealing and protecting microelectronic devices, such as semiconductor devices and other components, including interconnecting conductors, air bridges, inductors or capacitors, against damage or contamination from outside the device.

The packaging of semiconductor devices is conventionally carried out, whether in plastic or in ceramic packages, after the active circuit elements have been formed by semiconductor device processing. Individual pads on each die are bonded to the leads of the lead frame and the wired bonded lead frame and die are packaged. Such individual handling of dice in the fabrication of the devices is labor-intensive and thus undesirable.

High speed semiconductor devices often use air bridges to decrease the capacitance between metal lines and the silicon substrate. Air is an excellent dielectric and it is desirable to dispose air bridges between metal lines carrying high speed signals and the substrate.

While semiconductor devices are very small devices, miniaturization thereof is desirable but is adversely affected by the need to package the devices in a way that will protect them from damage or contamination. While encapsulation in plastic or ceramic provides suitable protection and isolation from contamination, the plastic or ceramic package is often many times the size of the semiconductor device and limits miniaturization thereof. In addition, plastic encapsulation may fill voids in the device, particularly voids that are provided for air bridges. The filling of these voids with plastic, which has a dielectric constant greater than air, increases the parasitic capacitance of the device and reduces its high frequency response limiting the speed at which signals can propagate in the device.

An object of the invention is to provide a device wafer with a plurality of device dice. A microelectronic structure, a micromachine, or a machinable component is formed in each device die. The device has contact pads to connect the device to external circuits and to power sources. Interconnects electrically connect surface contact regions of the device to the contact pads. A cover wafer is bonded to the device wafer. Vias extend from the outer surface of the device wafer, or the cover wafer, or both to the contact pads. In one embodiment, the vias terminate with bump contacts for connecting other devices or power sources to the packaged semiconductor device.

All processing is performed at the wafer level, including packaging, die identification, and testing. Semiconductor devices are formed in dice of a wafer of semiconductor material, such as silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or any other semiconductor known to those skilled in the art. The devices in the dice have surface contact regions for receiving interconnects to external devices and power supplies. Contact pads are formed within the dice and scribe trenches are formed between dice. Suitable interconnects are formed between surface contact regions of the dice and the contact pads. A cover wafer is bonded to the device wafer. The device wafer is thinned to open the scribe trench. The device wafer, the cover wafer, or both are processed to form vias to an outside surface of at least one of the cover or device wafers. Contact bumps are formed on the vias. The cov-

tested before they are separated from each other. The dice are separated from each other by thinning or scribing.

The present invention includes a packaged semiconductor device comprising a device die of semiconductor material having an inner surface and an outer surface, said inner surface having a plurality of contact pads and one or more devices formed in the inner surface, said devices each having one or more surface contact regions, an interconnect structure for electrically connecting the contact pads to the surface contact regions, a cover die having an inner surface and an outer surface with its inner surface bonded to the device die to cover the semiconductor devices, a plurality of conductive vias, each via extending from an outer end at the outer surface of the cover die to a contact pad on the device die, and an external contact on the outer end of each via.

The invention also includes a method for forming a packaged semiconductor device at the wafer level comprising the steps of:

in a device wafer of semiconductor material having an inner surface and an outer surface and divided into a plurality of dice, forming a device in each of said plurality of dice, each device having one or more surface contact regions,

forming contact pads for each device in the inner surface of the device wafer,

forming an interconnect between a portion of the contact pads and a portion of the surface contact regions of each device,

bonding an inner surface of a cover wafer having inner and outer surfaces to the device wafer for protecting the device,

forming a plurality of conductive vias, each via extending from one of the outer surfaces of one of the wafers to a contact pad on the inner surface of the device wafer,

forming on external contact on the outer end of each said via, and

separating the packagec die from each other to provide individually packaged devices.

The invention will now be described, by way of example, with reference to the accompanying drawings in which:

FIG. 1 is a cross sectional view of a device wafer with a scribe trenches and contact cavities;

FIG. 2 is cross sectional view showing the contact cavity filled with a metal;

FIG. 3 is a cross sectional view showing a dielectric layer with interconnects extending from contact pads on the semiconductor device to devices in the device wafer;

FIG. 4 is a cross sectional view of a cover wafer;

FIG. 5 is a cross sectional view of the bonded cover and device wafer;

FIG. 6 is a cross sectional view showing contact bumps and partial openings in the scribe trenches;

FIG. 7 is a completed device with contact bumps on the device wafer;

FIG. 8 shows an intermediate cross section of a second embodiment;

FIG. 9 is a third embodiment suitable for forming contact bumps on the cover wafer;

FIG. 10 is a cross section of a cover wafer;

FIG. 11 is a cross section of a cover wafer of FIG. 10 bonded to the device wafer of FIG. 9;

FIG. 12 shows a cross section of the cover with contact bumps and scribe trenches formed in the structure of FIG. 11;

FIG. 13 shows the separated die with contact bumps on the cover wafer;

FIG. 14 shows separated die with contact bumps on the cover wafer and the device wafer.

FIG. 1 illustrates device die 330 of silicon wafer 300. The die 330 has a plurality of contact cavities 352 that are distributed about the periphery of a device area 340, which will be processed to form one or more microelectronic structures including but not limited to transistors, resistors, diodes, capacitors, and inductors. The device area 340 may also be processed to form a micromachine such as a deformable mirror device, or a machinable component. Scribe trenches 348 are disposed spaced from the contact cavities 352. The depth of the scribe trench 348 and the depth of the contact cavity 352 will determine the final thickness of the device substrate 330. The depth of the contact cavities 352 is greater than the depth of the devices formed in device substrate 330. The scribe trenches 348 and contact cavities 352 are formed by masking the device wafer 300 with photoresist, patterning the resist to selectively expose the device substrate and etching the trenches 348 and cavities 352.

Next, the surface of device wafer 300 is masked and a layer of metal, preferably a refractory metal, is deposited in contact openings 352 to form contact pads 332, as shown in FIG. 2. It is preferable to use a refractory metal such as titanium or titanium tungsten, or a silicide because the substrate 330 will be heated to high temperatures during further processing.

The intermediate structure shown in FIG. 2, is processed to form a semiconductor device 340 as shown in FIG. 3. Details of the formation of the semiconductor device are not provided. However, any process including any suitable metal oxide semiconductor process, or bipolar process or BICMOS process may be used to form the semiconductor device 340. The semiconductor device 340 has one or more surface contact regions 210, 212. These surface contact regions connect the semiconductor device 340 to interconnect metal 338. A dielectric layer 354 of suitable material including but not limited to silicon dioxide or silicon nitride, is formed over the semiconductor device 340. The dielectric layer 354 has contacts 310-313 connecting the surface contact regions 210, 212 and the contact pads 332 to the interconnect metal 338. For example, openings for contacts are made in the dielectric layer 354. A metal, such as aluminum is deposited over the layer 354 to fill the contact openings. The deposited metal layer is patterned with photoresist and etched to form the interconnect metal layer 338. The thickness of dielectric layer 354 is increased to cover and enclose the interconnect metal 358. Dielectric layer 354 is further processed to provide further openings 356 aligned with scribe trenches 348.

Turning to FIG. 4, a cover wafer 360, typically formed of semiconductor material such as silicon, is provided with scribe trenches 358 that correspond to the scribe trenches of 348 of device substrate 330.

FIG. 5 refers to cover wafer 360 bonded to the device wafer 300. The inner surface of the cover substrate 360 is bonded to dielectric layer 354 of device wafer 300. The outer surfaces of both the device wafer 300 and the cover wafer 360 are available for further processing. FIG. 6 illustrates the device wafer 300 thinned by removing a portion of the device substrate material from the outer surface in order to expose the refractory metal 332 and the scribe trenches 348. The dice of wafer 300 are suitably marked with indicia to indicate, for example: manufacturer and type of device. A suitable marking method may be used, including but not limited to a laser marking tool or masking and etching, implanting or oxidizing that inscribes indicia, including but not limited to alpha-numeric characters, which are visible from the outer surface of each packaged die. The exposed contact pads 332 are treated with a customary bump process in order to form bump contacts 333 on the contact pads 332. The cover wafer 360 is either further thinned or scribed to separate the dice 330 in device wafer 300 from each other in order to provide the finished device as shown in FIG. 7.

FIG. 8 illustrates a second embodiment of the processing shown in FIG. 3. The structure shown in FIG. 8 does not require refractory metal for contact pads

331. Instead, the scribe trenches 348 and the contact cavities 352 are formed after the device 340 is completed. A metal or silicide 380 is formed in contact cavities 352 in order to form contact pads 331. Dielectric layer 354 is suitably patterned to provide openings to contact pad 331 and surface contact regions 210, 212. Next, a layer of metal is deposited over dielectric 354 to fill the openings. The metal layer is suitably patterned into interconnect 338. The thickness of the dielectric layer 354 is increased to enclose the interconnect 338. Dielectric layer 354 is further patterned and etched to provide scribe trenches 356. The intermediate structure shown in FIG. 8 is further processed to provide the device shown in FIG. 7.

FIG. 9 shows an intermediate stage in manufacturing a top bump contact device. There the dielectric layer 354 is formed over the device wafer 300. Openings to surface contact regions 210, 212 are made in dielectric metal is suitably patterned to form interconnects 338. The dielectric layer 354 thickness is increased to enclose interconnects 338. After the interconnects 338 are encased in dielectric, further openings 355 and 356 are made in the dielectric. Openings 356 are scribe openings; openings 355 expose the interconnect 338. As shown in FIG. 10, a cover substrate 360 having scribe trenches 358 and contact holes 357 is suitably bonded to the intermediate structure of FIG. 9 to provide the intermediate structure shown in FIG. 11. Next, cover wafer 360 is thinned to open scribe trenches 358 and holes 357 to interconnect 338. The via holes 355, 357 to interconnect 338 are filled with metal 372, and bump contacts 334 are formed on the outer surface of the cover substrate 360 as shown in FIG. 12. The die 330 is separated from adjacent devices with a saw or laser or diamond scribing tool or by etching wafer 300 in order to provide the structure shown in FIG. 13.

That device has bump contacts on the outer surface of the cover substrate 360 and on the device substrate 330. A plurality of devices of the type shown in FIG. 14 may be stacked to provide a module where interconnections are made both via the top and bottom surfaces through the respective bump pads 333 and 334, thereby providing a miniature module containing a plurality of semiconductor devices.

The advantages that are obtained in the various embodiments of the invention may be one or more of the following: (1) a die containing an semiconductor device that is thin for rapid heat flow; (2) metal point or bump interconnections which permit smaller die areas than tab bonding as well as better thermal and electrical transmission properties than tabs; (3) all processing before separation into dice may be carried out at the wafer level; (4) chemical thinning and separation of wafers and dice may be used if desired; (5) polymers such as PMMA or similar organic compounds and other low temperature plastic bonding materials may be used to bond the wafers into packaged assemblies providing the semiconductor devices; (6) the dice (the final devices) need not be rectilinear but may be of other shapes and/or have rounded corners; (7) dice may be identified by etching into the top or bottom surfaces of the substrates before separation; (8) package level contact pads are accessible at the wafer level to enable wafer level burn-in of the semiconductor devices and final test thereof while still in wafer form thereby eliminating final package tests; (9) a conventional scribe and break process provides the final package assembly; (10) individual die mounting, bonding, encapsulation and branding may be eliminated; (11) the wafers and the dice may be handled by automatic robotic machinery; (12) since the dice are handled at the wafer level, mechanically induced defects are eliminated (for example chips hitting each other cause edges to be knocked off), improving the yield in the number of packaged die per batch over yields needing conventional die handling [illegible] (13) the final encapsulated die has the

For an air bridge, a cavity is formed in the surface of the device wafer and air bridge conductors transit the cavity. The cavity may contain other devices, including but not limited to resonant beams, photodetectors, surface acoustic wave devices, moveable mirror devices, and other micromachines. The cover wafer may be made of semiconductor material or any other material suitable for processing and packaging. In addition, the cover wafer may be transparent or opaque to light. A transparent cover wafer is preferred for photodetector devices and other devices such as erasable programmable read only memory (eprom) devices that are erased by exposing the memory device to ultraviolet radiation. If the cover wafer is made of silicon, it can be rendered transparent by oxidizing the cover wafer to convert the silicon into transparent silicon dioxide.

Semiconductor devices 340 are formed in semiconductor wafer 300. Contact pads 332 are formed in each die 330. An interconnect connects the contact pads 332 to die surface contact regions 210, 212. Scribe trenches 348 are formed in device wafer 300; corresponding trenches 358 are formed in cover wafer 360. The cover wafer 360 is thinned to open scribe trenches 348. Conductive vias 310-313 connect the contact pads 210, 212 to external surface bump contacts 333.

Claims

1. A packaged semiconductor device comprising:

   a device die of semiconductor material having an inner surface and an outer surface, said inner surface having a plurality of contact pads and one or more devices formed in the inner surface, said devices each having one or more surface contact regions;

   an interconnect structure for electrically connecting the contact pads to the surface contact regions;

a cover die having an inner surface and an outer surface with its inner surface bonded to the device die to cover the semiconductor devices;

a plurality of conductive vias, each via extending from an outer end at the outer surface of the cover die to a contact pad on the device die; and

an external contact on the outer end of each via.

2. A semiconductor device as claimed in claim 1 characterized by dielectric layer formed over the inner surface of the device die, said dielectric layer including said interconnect and the external contact comprises a bump contact raised from said surface.

3. A semiconductor device as claimed in claim 1 or 2 wherein the vias extend to the outer surface of the device die, or the vias extend to the outer surface of the cover die, and preferably in which the vias extend to the outer surface of the device die and the outer surface of the cover die.

4. A semiconductor device as claimed in claim 1, 2 or 3 wherein device die or the cover die is one semiconductor material selected from the group consisting of silicon, germanium, silicon germanium, silicon carbide, and gallium arsenide.

5. A semiconductor device as claimed in any one of claims 1 to 4 wherein said device die comprises a cavity, in which said cover die is opaque, or said cover die is transparent, or said cover die comprises transparent regions and opaque regions.

6. A method for forming a packaged semiconductor device at the wafer level comprising the steps of:

in a device wafer of semiconductor material having an inner surface and an outer surface and divided into a plurality of dice, forming a device in each of said plurality of dice, each device having one or more surface contact regions;

forming contact pads for each device in the inner surface of the device wafer;

forming an interconnect between a portion of the contact pads and a portion of the surface contact regions of each device;

bonding an inner surface of a cover wafer having inner and outer surfaces to the device wafer for protecting the devices;

forming a plurality of conductive vias, each via extending from one of the outer surfaces of one of the wafers to a contact pad on the inner surface of the device wafer;

forming on external contact on the outer end of each said via, and

separating the packaged die from each other to provide individually packaged devices.

7. A method as claimed in claim 6 characterized by forming a dielectric layer over the inner surface of the device wafer, forming a plurality of via openings through the dielectric layer to the contact pads and to the surface contact regions, forming a conductive layer on the dielectric layer and in the vias, patterning the conductive layer into an interconnect for connecting the contact pads to the surface contact regions, covering the interconnect with dielectric.

8. A method as claimed in claims 6 or 7 as characterized by forming conductive vias in the outer surface of the device wafer to the contact pads, or forming conductive vias in the outer surface of the cover wafer to the contact pads, or forming conductive vias in the outer surface of the device wafer and in the cover wafer.

9. A method as claimed in claims 6, 7 or 8 wherein the device wafer or the cover wafer comprises one material selected from the group consisting of silicon, germanium, silicon germanium, silicon carbide, and gallium arsenide.

10. A method as claimed in claim 9 characterized by forming scribe trenches in the inner surface of said device wafer, and cover wafer, and including the step of marking indicia visible from the outer surface of each covered die before separating the dice from each other, and preferably electrically testing the dice after the dice are covered but before they are separated from each other.

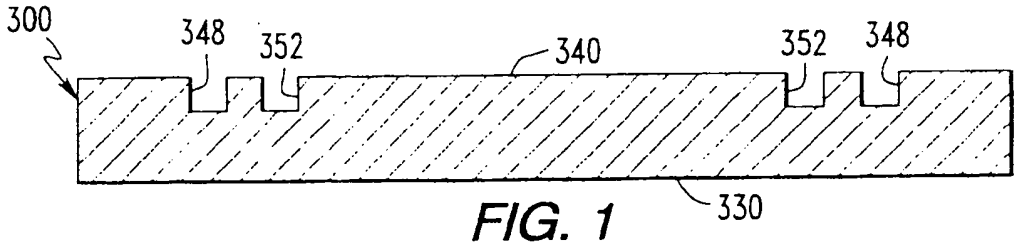

FIG. 1

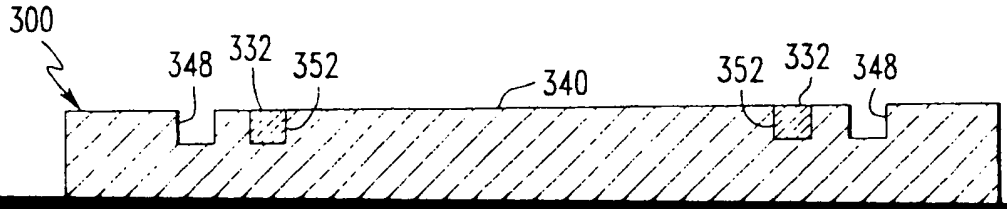

FIG. 2

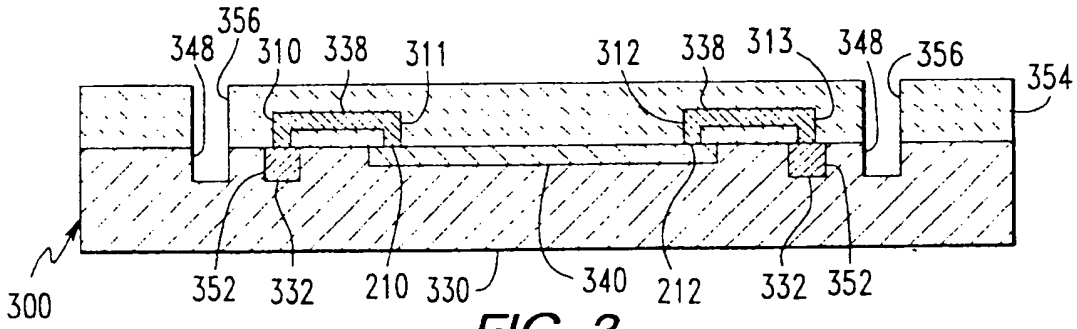

FIG. 3

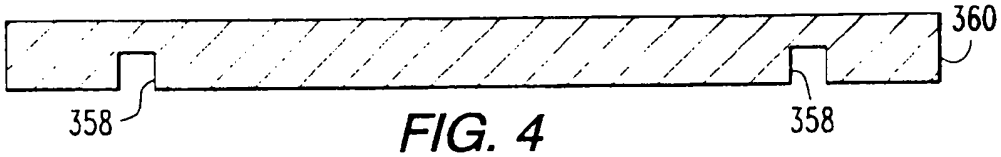

FIG. 4

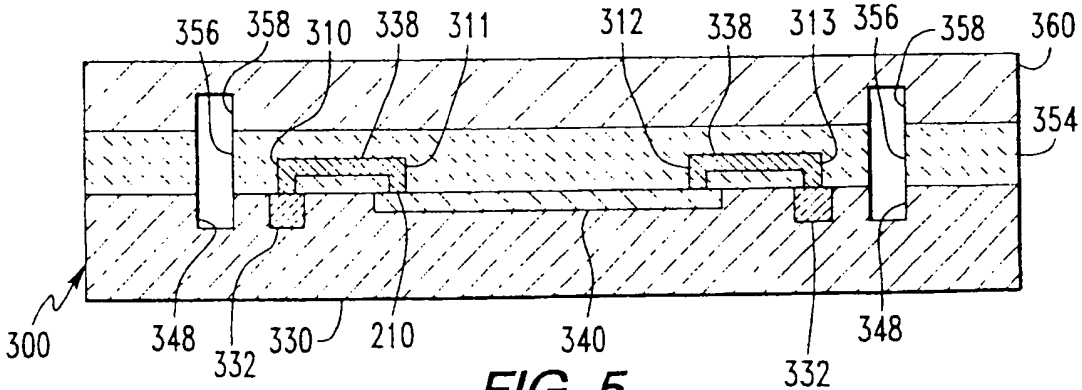

FIG. 5

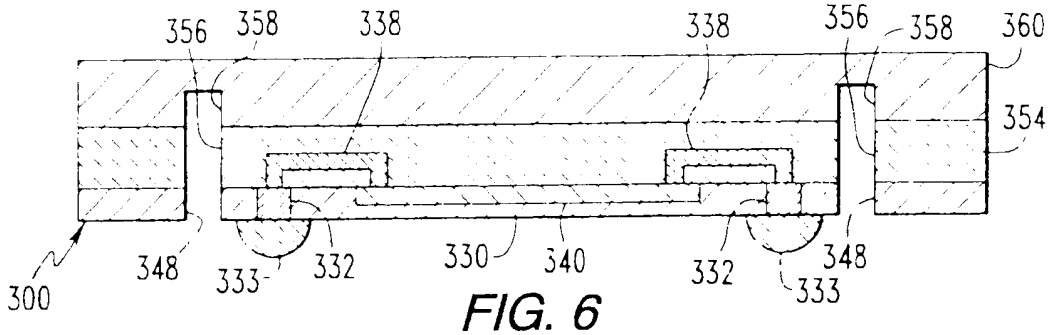

FIG. 6

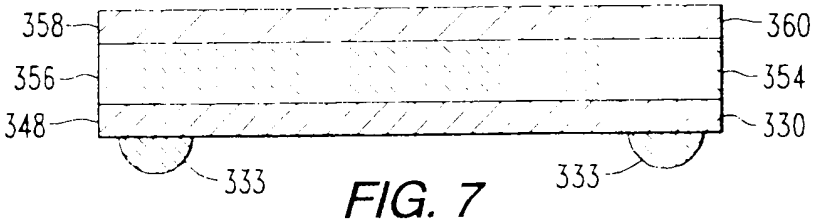

FIG. 7

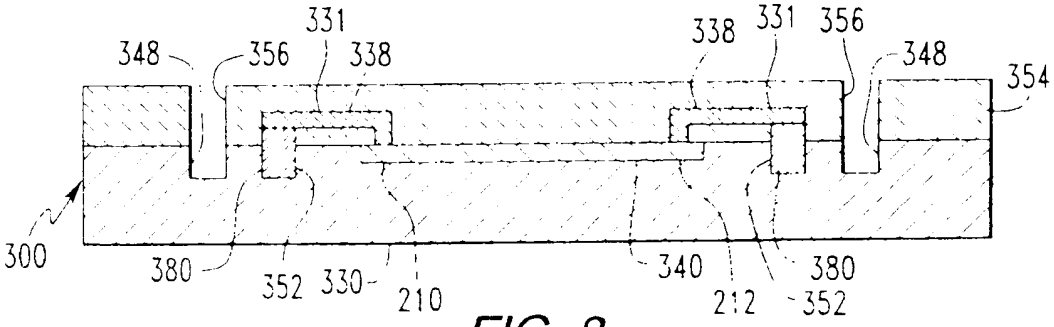

FIG. 8

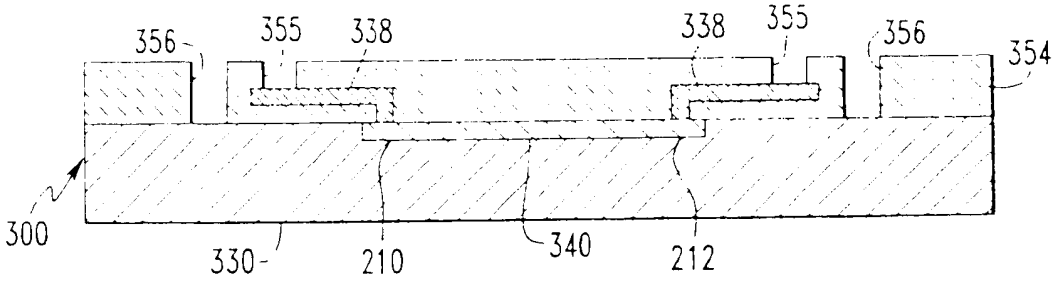

FIG. 9

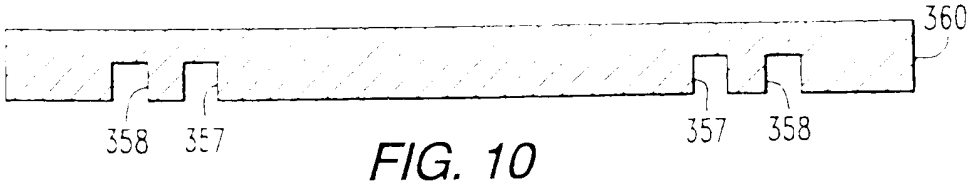

FIG. 10

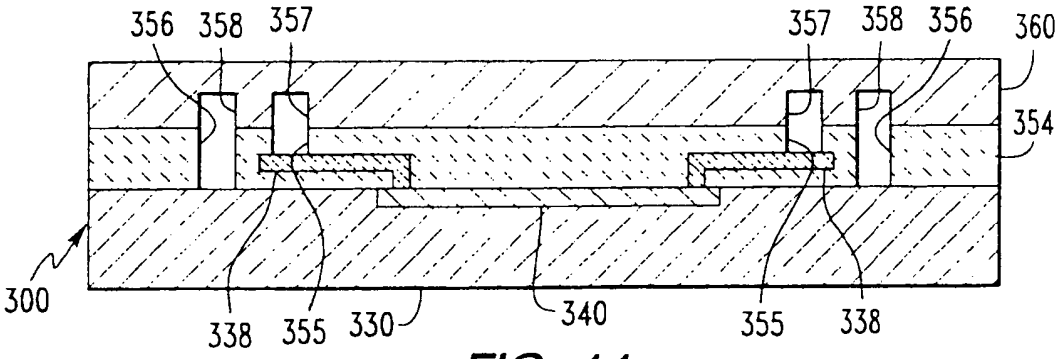

FIG. 11

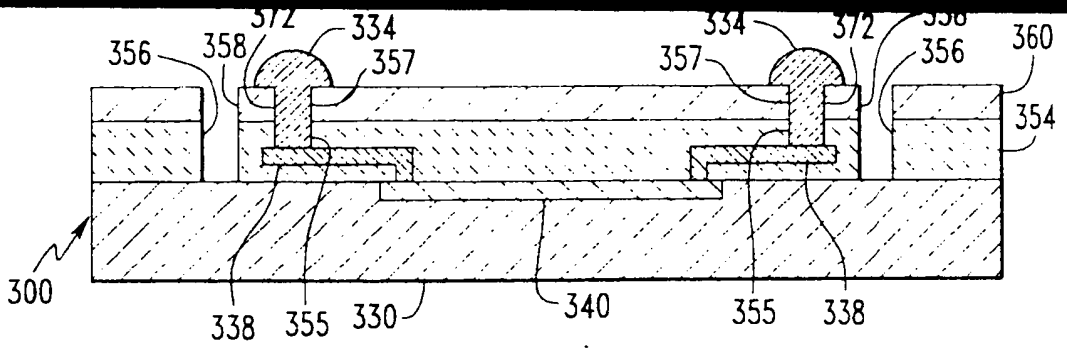

FIG. 12

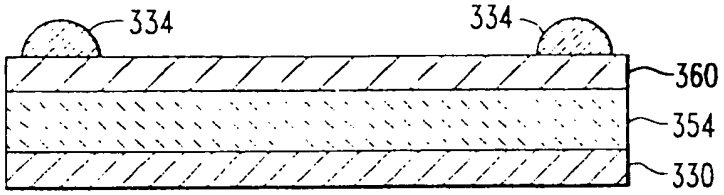

FIG. 13

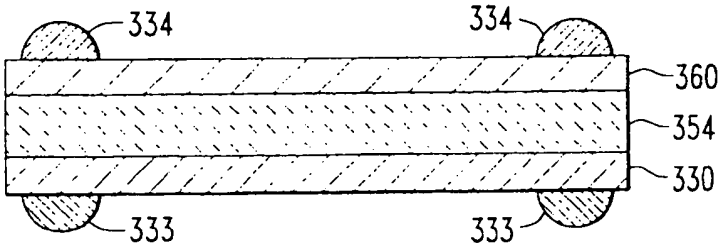

FIG. 14

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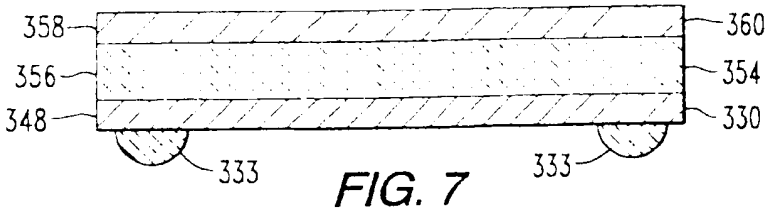

FIG. 7

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 10 7670

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 196 (E-755), 10 May 1989 -& JP 01 018248 A (NEC CORP), 23 January 1989 * abstract *	1,3,4,6, 8,9	H01L23/485 H01L23/48 H01L21/304
X	US 5 481 133 A (HSU CHEN-CHUNG) 2 January 1996	1,3,4, 6-9	
X	EP 0 635 885 A (HUGHES AIRCRAFT CO) 25 January 1995 * column 3, line 51 - column 8, line 8; figures 1C,3 *	1,3,4,6, 8,9	
X	EP 0 684 643 A (KONINKL PHILIPS ELECTRONICS NV) 29 November 1995 * column 4, line 35 - column 6, line 57; figure 6 *	1,3,5-9	
Y		2	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
X	EP 0 316 799 A (NISSAN MOTOR) 24 May 1989 * column 4, line 18 - column 6, line 55 * * column 11, line 53 - column 12, line 16; figure 6 *	1,3,4, 6-9	H01L
Y	PATENT ABSTRACTS OF JAPAN vol. 014, no. 166 (E-0911), 30 March 1990 -& JP 02 023623 A (SHARP CORP), 25 January 1990 * abstract *	2	
A	US 5 343 064 A (SPANGLER LELAND J ET AL) 30 August 1994 * column 10, line 4 - column 18, line 42; figure 8 *	1,4-7,9	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	8 June 1999	Edmeades, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

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EPO FORM 1503 03.82 (P04C01)

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08-06-1999

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